What is Claimed is:

1. A system for connecting a set of device chips by attaching them by means of a microjoint structure comprising:

a microjoint chip carrier including a multilayer substrate having a plurality of receptacles in its top surface;

a set of microjoint pads on the device chips that match the said receptacles, and

interconnect wiring in the carrier connecting the carrier receptacles so as to allow the interconnection of device chips.

2. A system as defined in Claim 1 wherein the pads on the device chips are formed to have studs extending from the top surface.

3. A system as defined in Claim 1 wherein the interior of the receptacles in the carrier are lined with contiguous layers of liner, seed, barrier metal and noble metal films.

4. A system as in Claim 3 wherein the liner layer is selected from the group consisting of W, Ta, Ti, WN, TaN, TiN, Cr or combinations thereof.

5. A system as in Claim 3 wherein the seed layer is copper.

6. A system as in Claim 3 wherein the barrier layer is selected from the group consisting of Ni, Co, Pt, Pd, Ni-P, Co-P, CoWP,

7. A system as defined in Claim 1, wherein the carrier includes a layer of silicon and a dielectric layer, the receptacles being in the dielectric layer, and the carrier wiring being below the dielectric layer.

8. A system as defined in Claim 3, wherein the liner layer initially extends over the dielectric layer and into the receptacles, but is then limited to the receptacles.

9. A system as defined in Claim 3, wherein the seed layer is limited to the receptacle.

10. A process for interconnecting a set of device chips by attaching a microjoint structure comprising:

forming the microjoint structure by building a carrier in the form of a multilayer substrate having a plurality of receptacles in its top surface;

forming a set of pads with studs extending outwards from them on the device chips;

matching and joining the pads on the device chips to the receptacles on the carrier, and

forming interconnect wiring that connects the carrier receptacles.

11. A process as defined in Claim 10 including the step of forming pads at the ends of studs extending from the semiconductor wafer.

12. A process as defined in Claim 10 including the step of forming contiguous layers of tantalum, copper and nickel at the peripheries of the receptacles in the top surface of the carrier.

13. A process as defined in Claim 10, wherein the carrier includes a layer of silicon and a dielectric layer, the receptacles being in the dielectric layer, and the carrier wiring being below the dielectric layer.

14. A process as defined in Claim 11, including the step of etching away the tantalum layer from the top surface of the dielectric layer.

15. A process in accordance with Claim 11, including the step of etching away the copper from the top surface of the dielectric layer.

The invention having been thus described with particular reference to the preferred forms thereof, it will be obvious that various changes and modifications may be made therein without departing from the spirit and scope of the invention as defined in the appended claims.